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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,582	06/04/2001	Mukesh K. Puri	1003-0558	2635

7590 05/18/2006

Intellectual Property Department
LSI Logic Corporation
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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,582	PURI ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8-17-05

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 September 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on February 28, 2006, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Arguments

Claim Rejections - 35 USC § 112

Applicant argues *... the examiner stated, "[I]t is not clear how testing is preformed by merely loading the output register and reloading the shift registers".*

The Examiner voices concerns that there is "no test data applied and no criteria listed for passing or failing data", and that there is "operational verification" of the memory circuit'.

Applicant further argues, *"The Claims do not require the Additional Limitations Identified by the Examiner"*

"Applicants submit that the independent claims are sufficiently definite, and that the preambles are not inconsistent with the bodies of the claims. The test under 35 U.S.C.112, second paragraph, is whether one of ordinary skill in the art would be able to determine the metes and bounds of the claimed property. Independent claims 1 and 11 have a readily determinable scope."

For example, claim 1 is directed to a circuit configuration for testing a semiconductor memory that includes an output register, a plurality of shift registers and means for selecting one of the plurality of shift registers for outputting digital data to the output register. The limitations of the output register, the shift register and the selection means, and there interrelationship, are readily understood. Moreover, such elements may readily form a circuit configuration for testing a semiconductor memory as claimed. Whether or not the preamble is read as a claim limitation, which in the case of claim 1 is not necessary, the scope of the entire claim is readily determined.

The examiner would like to point out that it is not obvious from the claim language that this circuit would be used as a part of a test circuit or in the function of a test circuit. One of ordinary skill in the art would be well aware that shift registers and output registers are used for other purposes than testing such as normal operation of a circuit. Often the test circuitry is used in normal operation and in testing.

Applicant also argues, "*With respect to claim 11, the method includes ". . . outputting digital data from a shift register into an output register" and "examining the*

digital data in the output register". It is unclear how this could be interpreted to be at odds with the preamble, "a method for testing a semiconductor memory". Specifically, the claimed test method includes moving data between registers, and then examining the data after it has been moved. Claim 11 clearly describes the steps of a test."

The examiner would like to point out that 'moving data between registers' does not constitute nor does it imply testing is being preformed. It is also not clear how data in the output register can be examined while it is in the output register as the drawings show only an output register (and make mention of an output pin being strobed only in the flowchart) and the specification does not explain this issue.

With regard to the Examiner's specific concern that there is "no test data applied and no criteria listed for passing or failing data", it is submitted that such information is not required to understand the metes and bounds of the invention. Moreover, claim 1 does indeed recite "output the digital data", and claim 11 does indeed recite "outputting digital data".

With respect to this the examiner again would like to point out that 'moving data between registers' does not constitute nor does it imply testing is being preformed. It is also not clear how data in the output register can be examined while it is in the output register as the drawings show only an output pin and the specification does not explain this issue.

Thus, even though a recitation of "test data" is not necessary, claims 1 and

11 appear to claim at least some "data" that is used in a "test" method or apparatus. With regard to the Examiner's concern that there is "no criteria listed for passing or failing data", it is submitted that the evaluation of the results of the test is not a precondition for performing a test. In other words, evaluation of test results necessarily implies that the test has been completed prior to evaluation.

By way of example, a common test in the electrical arts involves placing a voltage on a circuit input and then measuring the circuit's output voltage. The test results may then be evaluated, but the performance of the test itself does not require evaluation of the results, and certainly does not require an evaluation as to whether pass and fail criteria are met. With regard to the "operational verification of the memory circuit, it is again submitted that the scope of claims 1 and 11 may readily be determined without reciting "operational verification of the memory circuit".

The IEEE dictionary (2000) defines test as "a set of stimuli, either applied or known, combined with a set of observed responses and criteria for comparing these responses to a known standard" or "an observed activity that may be caused to occur (e.g., stimulus-response) in order to obtain information about the behavior of a test subject". Therefore a person having ordinary skill in the art would expect a test to have test data and at least some form of test data (stimulus/response).

Claims 2-10 and 12-16 are dependent on the independent claims 1 and 11 and therefore inherit the 3 USC 112 rejections of the independent claims as recited previously, and may not be further considered on the merits with respect to the art.

Therefore, the examiner maintains the previously presented 35 USC 112, second paragraph rejections of claims 1-16.

Applicant's arguments with respect to the art rejections of claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mollier U.S. Patent No. 4,344,155 in view of Kuijk U.S. Patent No. 4,584673.

As per claims 1 and 11, Mollier substantially teaches the claimed circuit configuration, in which a plurality of shift registers for serially outputting the digital data to be received by the output register, wherein each of the plurality of shift registers includes a feedback path for enabling the digital data output by each individual register of the plurality of shift registers to be input back into the same individual register in a same sequence as the digital data is output from the same individual register (Column 6 line 62 through column 7 line 11). Not disclosed by Mollier is the plurality of registers and means for selecting which register to output.

However, in an analogous art, Kuijk teaches a plurality of shift registers in which the output to the register is determined by a selector circuit (Figures 4 and 5, column 8 line 30 through column 9 line 50) therefore it would have been obvious to a person having ordinary skill in the art to have used the feedback configuration of Mollier with the selectors of a plurality of registers as taught by Kuijk. This would have been obvious to a person having ordinary skill in the art in order to use fewer output points with a large number of registers.

As per claims 2-5 Kuijk teaches the creation of dummy bit positions hence the ability to make a register as long or as short as necessary for a specific application. (column 9 line65 through column 10 line 5)

As per claims 6 and 7, a plurality of shift registers being output to an output register, would have been obvious to a person having ordinary skill in the art at the time this invention was made in order to make sure that the output register would be large enough to hold the amount of data that would be sent, and that at some point the output would be strobbed in order to collect the data. This would have been obvious because a person having ordinary skill in the art would want to access all of the data that had been collected.

As per claim 8, Kuijk teaches selector element (switch or multiplexer) in order to clock the data out of the plurality of registers (figures 4 and 5)..

As per claims 9, 13, and 16, the examiner would like to point out that the prior art is replete with references having shift registers connected within BISR memory arrays (see cited references on form 892) and it would therefore be obvious to a person having ordinary skill in the art at the time this invention was made to have used this as a design choice based on the intended use of the circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

The examiner invites applicant to call and arrange an interview in which acceptable wording of the claim language can be determined in order to speed up the prosecution and possible allowance of this case,

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2138

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